Subject Code: XXXXX

Roll No:

BTECH

(SEM-7) VLSI DESIGN 2021-22

TIME:3 HOUR ***Total Marks: 100***

Instruction: Attempt the questions as per the given instructions. Assume missing data suitably.

SECTION - A

Attempt *All Parts* in Brief **2*10 = 20**

Q1	Questions	Marks
(a)	What is Photolithography ?	2
(b)	Why we need a low power VLSI circuits in today's scenario ?	2
(c)	What is contamination delay ?	2
(d)	Define logical effect with example.	2
(e)	Differentiate between static power and dynamic power.	2
(f)	Implement 2 : 1 MUX using CMOS transmission gate.	2
(g)	Describe different storage elements.	2
(h)	Distinguish between SRAM and DRAM.	2
(i)	Explain the term controllability and observability.	2
(j)	What is meant by Stuck-at-1 fault and Stuck-at-0 fault ?	2

SECTION - B		
Attempt *Any Three* of the following		**3*10 = 30**
Q2	**Questions**	**Marks**
(a)	Discuss the hierarchy of various semiconductors with Moore's law. Write short note on VLSI testing.	10
(b)	Explain Elmore delay model with suitable RC networks. Mention its merits.	10
(c)	Compare the performance of Domino CMOS logic and NP Domino CMOS logic with suitable example.	10
(d)	Explain read/write operation of SRAM memory cell. How 1 bit cell is used in bigger memory systems.	10
(e)	Explain the issues involved in BIST techniques in details.	10

SECTION - C		
Attempt *Any One* of the following		**5*10 = 50**
Q3	**Questions**	**Marks**
(a)	Draw the Y-chart and explain VLSI design process. Mention its advantages.	10
(b)	Explain the CMOS fabrication steps with neat diagram using n-well process.	10
Q4	**Questions**	**Marks**
(a)	Derive the expression for total power dissipation of a CMOS circuit.	10
(b)	Draw and explain the working of RC delay model for interconnects.	10
Q5	**Questions**	**Marks**
(a)	Draw and explain NORA and TSPC dynamic CMOS logic.	10
(b)	What is pre-charge evaluate logic in dynamic CMOS logic and draw the basic architecture of SRAM and DRAM.	10
Q6	**Questions**	**Marks**
(a)	Write short note on DRAM cell. Explain leakage and refresh operation in DRAM cells.	10
(b)	Explain the various types of power dissipation in CMOS circuits.	10
Q7	**Questions**	**Marks**
(a)	Explain the parallel procession approach in low power CMOS circuits.	10

(b)	Write a short note on : i. Adiabatic logic circuits ii. Sean cell based approach.	10